RTDS Technologies

PRODUCT PROFILE

MMC Modelling

Modular Multilevel Converters (MMCs) offer many advantages over conventional thyristor-based schemes and are becoming widely used in HVDC and FACTS applications. They also present significant challenges for modelling with Electro-Magnetic Transient (EMT) simulation techniques. RTDS Technologies has developed a number of models to overcome these challenges. These models are small timestep sub-network components which allow great flexibility of configuration as well as very low loop delay between the real time simulation and external controls.

GTFPGA Unit: Powerful, dedicated hardware

The GTFPGA Unit is a hardware component used for modelling the FPGA-based MMC models available in the RSCAD software. Each Unit is rack mountable, and houses an FPGA board. The Unit can be used to model MMC-based valves or capacitor voltage balancing and firing pulse control for MMC-based valves. The FPGA board can also be used as a generic interface to the RTDS Simulator by using the GTFPGA netlist. Due to the powerful computation capabilities of the FPGA board, it can run more detailed MMC models in real time compared to the rack-mounted processor cards.

The options for modelling MMC-based valves on the GTFPGA Unit are described below.

Previously, it was called the MMC Support Unit. Today, it's the GTFPGA Unit, and supports more functionality than ever.

FPGA-Based Models

The following models have been developed for execution on the Xilinx FPGA board within the GTFPGA Unit. These components are fully integrated into RSCAD's small timestep subnetwork, providing valuable modelling flexibility. They are designed to test detailed firing pulse controls and are widely used for Factory Acceptance Testing of MMC-based HVDC and FACTS controls. NovaCor or PB5 cards are required to interface the FPGA-based MMC models to.

Unified Model (U5)

Using U5, the user can model up to 6 valve legs on one GTFPGA Unit. Each valve leg can include up to 512 submodules (SMs). Both half and full bridge configurations are supported. Normal firing states are considered (blocked, positive inserted, negative inserted, and bypassed). Internal faults can be simulated, but not at the IGBT level. Supports the addition of a damping SM.

Generic Model (GM)

The GM involves a higher calculation density—the user can model up to 2 valve legs on one GTFPGA Unit. Each valve leg can include up to 1024 SMs. Half bridge, full bridge, and mixed configurations are supported. All possible IGBT firing states are considered. The GM supports individual IGBT firing, individual SM capacitances, customized topologies, and internal valve to ground faults. Supports the addition of a damping SM.

Processor-Based Models

The following models have been developed for execution on either a GPC or PB5 processor card.

MMC5

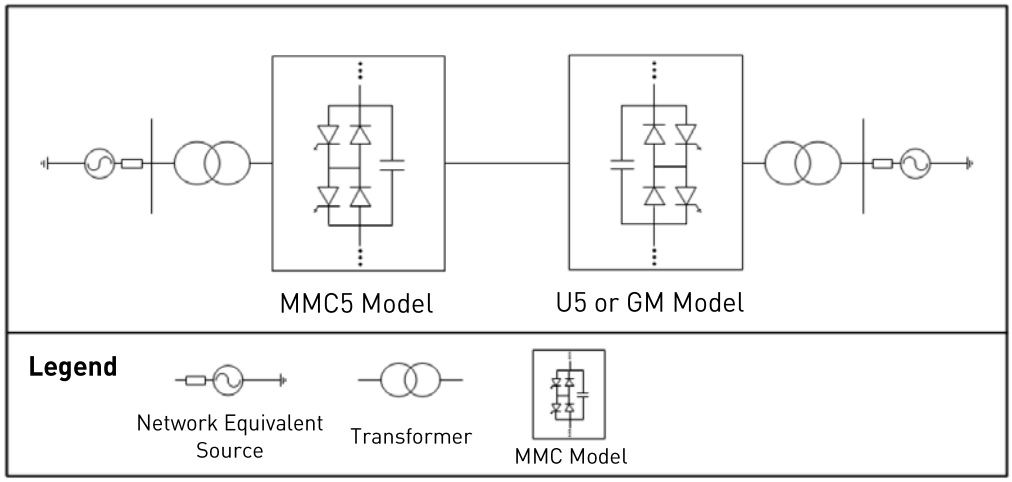
The MMC5 component is designed for the testing of high level controls and system performance. Three valve legs can be simulated on one processor. Each valve leg can have up to 640 submodules. Both full and half bridge configurations are supported. Ideal capacitor voltage balancing is provided internally by the model. At the end of each small timestep, all submodules arrive at the same average capacitor voltage.

CHAINV5

The CHAINV5 is a processor-based model that supports individual submodule firing pulse input, and can be used to test detailed firing pulse controls. CHAINV5 can model 40 submodules per valve for a full bridge configuration, or 56 submodules per valve for a half bridge configuration. The simulation of internal faults is not permitted when using CHAINV5.

Implementation Example

The following sample case is available in RSCAD. It demonstrates a two-terminal HVDC scheme employing MMCs. The MMC valves involved each contain 512 submodules. The valves at one end of the scheme are modelled using the MMC5 processor-based component, while the valves at the other end are modelled in full detail using the U5 FPGA-based component. The GM could also be used to model the valves at the FPGA end.



Using the U5 model, one GTFPGA Unit can represent all six FPGA-based valve models involved. Using the GM model, which is more detailed and has a higher calculation density, three GTFPGA Units can represent the FPGA-based valves. In both cases, two other GTFPGA Units can provide the capacitor voltage balancing and firing pulse control for the terminal. The user can implement their own controller or use an optional generic controller available in RSCAD.

The high level control for the HVDC scheme is represented using PB5 processors.

As mentioned above, not only are six MMC valves represented using GTFPGA Units, but also their respective capacitor balancing and firing pulse controls. The GTFPGA Units representing the valves are connected to the GTFPGA Units containing the firing pulse controls via optical fibre. The valve models calculate the valve current and the capacitor voltage for each submodule and send the information to the controller. The control in turn provides the firing pulses for each submodule. The signal exchange uses a standard high-speed serial protocol, Aurora, which can be adopted and used for the connection of any external controller.

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