Co-simulation of an FPGA-based Electromagnetic Transient Model and a Small Time-Step Model in the RTDS Real-Time Digital Simulator

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Abstract
This paper describes work in electromagnetic transient co-simulation of a field-programmable gate array (FPGA)-based model with an RTDS Real-Time Digital Simulator. Results are presented toward achieving the goal of simulating high-frequency power electronic converters in real-time co-simulation with a rest-of-system transient model. Power system converter models using the RTDS were previously implemented at rates up to approximately 6 kHz switching frequency using voltage source converter models in a small time-step of ~1.5-2 µsecs. In this work, the FPGA-based transient simulation models of a static and switched RL load are interfaced to the RTDS small time-step model through a traveling wave model. The high-frequency switching models suggest the feasibility of FPGA-based simulation of a high-frequency switching converter.

1. INTRODUCTION

The real-time computer simulation of complex electrical systems has proven to be a highly useful technique for dynamic testing of physical devices. This method of hardware-in-the-loop (HIL) simulation provides greater understanding and de-risking of the development of devices before field insertion. The physical hardware interacts in real-time, via analog and digital signals, with a rest-of-system model that is simulated in software. This HIL simulation provides a realistic operating environment for the physical device. At the same time the computer simulation receives system information from the real-world device which propagates into the real-time simulation in a closed loop. HIL simulation may consist of a physical controller interacting with the simulated mode, known as controller hardware-in-the-loop (CHIL), or may include a power device under test, with appropriate amplifiers and sensors, which may be known as power hardware-in-the-loop (PHIL) simulation.

For the real-time modeling of voltage source converters (VSC), the time-step required and the necessary interfacing to the controller presents a challenge to the researcher. A common method used in real-time simulation systems is to use tightly linked multi-rate co-simulations, with part of the simulation running at one time-step, and a more time-critical part of the simulation running at a faster time-step. Since VSC modeling is desired in high-fidelity simulations, and the switching frequencies of these controllers continue to increase, new simulation techniques must be developed to meet the challenge.

The Real-Time Digital Simulator (RTDS) by RTDS Technologies, Inc. [1] is widely used for real-time simulations and HIL applications. In this simulation system, the main electrical network and necessary control systems are simulated with a typical time-step size of about 50 µs. VSC simulation is achieved by dedicating a separate processor for small time-step simulations, with a time-step size of 1.4 to 2.5 µs. The VSC simulation can be pure software, with internally generated switching pulses, or the simulator may be connected to a physical controller, which generates firing pulse voltages that are input to the RTDS small-time-step simulation. This method allows simulation of converters with switching frequencies up to about 6 kHz. The present work is motivated by a need to simulate converters with higher switching frequencies.

2. SIMULATION EQUIPMENT

A real-time simulation capability with an integrated 5 MW test facility has been established at the Center for Advanced Power Systems (CAPS) at Florida State University [2]. The integration of the facility equipment with an RTDS real-time digital simulator has allowed dynamic simulation and test procedures in a variety of HIL experiments, as well as simulation model development and validation. The RTDS at CAPS is a multi-processor machine, with 150 processors, including Analog Devices ADSP21062, IBM PPC750GX, and Freescale MC7448. Dedicated digital and analog input/output cards are connected via a 2 Gbps fiber interface to a subset of these processors.

The fiber protocol implemented between the I/O cards and the processor cards is a low-latency, high-throughput protocol that is synchronized to the simulator time-step start, for either the large or small time-steps. Since the data carried on this fiber link are in digital format with high bit resolution and very low noise, a proposal was made to
RTDS Technologies in 2009 to make the protocol details available to end users for the purpose of implementing a user-specified interface card. Since this method would involve a complete disclosure of the RTDS interface protocol, and possible re-implementation after any future protocol changes, an alternate method was made available by RTDS Technologies [3].

The Xilinx ML507 evaluation platform, which is based on a Virtex 5 field programmable gate array (FPGA), is used to interface to the RTDS fiber I/O data protocol. This card, referred to as the GTFPGA, includes hardware I/O ports and an embedded RISC processor. A necessary software component is an “interface module” netlist provided by RTDS Technologies. This module encodes and decodes the optical signal, and provides for bi-directional transfer of up to 64 values in each direction per simulation time-step—either 32-bit floating point or integer. The design of the VHDL is entirely up to the researcher according to the needs of the project.

The GTFPGA has been used for several real-time projects at CAPS and results have been reported for a low-latency, multi-lane communication demonstration reported in [4], and a wavelet-based power quality analysis in [5]. These and other efforts have been focused on control signal interfacing at the RTDS large-time-step boundary.

3. POWER SIMULATION AND ANALYSIS

In contrast to the former control signal interface projects, a new small-time-step model (ie. 1.5 – 2.5 µs time-step size) has been introduced as a prototype model that allows electrical power flow to the FPGA subsystem by means of bi-directional current injections through a simulated Bergeron transmission line model. Figure 1 schematically shows the design architecture of such a co-simulation using the CAPS RTDS and GTFPGA subsystem. One half of the transmission line is modeled in the RTDS and the other half is modeled in the FPGA.

As an initial demonstration, a transient power simulation using the Dommel algorithm [6] was coded for the FPGA for an RL load (R=0.5 Ω, L=1.33e-3 H), with transmission line parameters of the same R and L values. The demonstration FPGA model and RTDS case were created by RTDS Technologies and provided to CAPS. The FPGA model calculates the current injections for the co-simulation interface, using a 2 µsec time-step equal to the RTDS small time-step. A circuit diagram for this simulation is shown in Figure 3.

To validate this FPGA-based calculation, a comparison simulation was made at CAPS with two interfaced small-time-step models, one consisting of an equivalent voltage source, and another consisting solely of the RL load, with a fiber connection between the processor nodes and a short (Bergeron) transmission line model connecting these nodes. Refer to Figure 2 and to Figure 3. The source in each model was a 60 Hz single phase voltage with a 60 Hz magnitude of 1.000, and the expected fundamental component of the current is 0.7071 A in both instances (to 4 significant figures). Table 1 shows the calculated deviation using available precision.

![Figure 2. Process model of electrical power flow for validation case using two RTDS small-time-step models.](image)

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<th>Deviation</th>
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Table 1. Deviation of FPGA-based model from validation model

Figure 1. Process model of electrical power flow between RTDS small-time-step model and FPGA-based electrical model.
4. FPGA LOAD SWITCHING SIMULATION

The FPGA offers specific increased capabilities due to its parallel computational capability and to its fast clock-cycle. The FPGA algorithm can thus execute faster than the RTDS small time-step, creating in effect the opportunity for a “very-small-time-step.” In this example above, the algorithm executes in 300 ns and then waits for the beginning of the next RTDS small time-step and bi-directional current exchange, showing the possibility of multiple time-steps inside the RTDS small time-step. The I/O pins on the FPGA are clocked at 100 MHz as well, and subject to signaling impedance, allow for rapidly changing inputs that could be used to resolve high-frequency PWM signals.

To demonstrate this capability, researchers at CAPS devised an FPGA-based electrical model that switches between two RL loads at a PWM-determined rate. The loads are $R=0.5 \, \Omega$, $L=1.33e-3 \, H$, and $R=0.1 \, \Omega$, $L=1.33e-3 \, H$. In this model, the voltage source is 1 kV DC.

![FPGA or RTDS processor](image)

Figure 3. Circuit diagram of Section 3 simulation.

Figure 4. Process model of FPGA-based PWM switched load.

The RL loads are first switched with the duty cycle indicated by Figure 5, and then with the duty cycle indicated by Figure 6. We demonstrate fast switching here, but the time-step is still 2 $\mu$s, and synchronized to the RTDS. Implementation of a “very-small-time-step” on the order of hundreds of nanoseconds is left for future development. Figure 7 captures the current increase when the duty cycle changes.

![Figure 5. PWM Duty Cycle 1.](image)

Figure 5. PWM Duty Cycle 1.

![Figure 6. PWM Duty Cycle 2.](image)

Figure 6. PWM Duty Cycle 2.
5. CURRENT INJECTION FUNCTION

The strategy of implementing a multi-switch converter, such as a DC-DC, dual active bridge, phase-shift control converter, seems possible by implementing the Dommel algorithm on the FPGA. For fast switching, it would be necessary to use a technique that avoids recalculation of the network matrix, such as that described in [7] or the use of multiple pre-calculated matrices. The magnitude of the necessary FPGA code should be considered, however.

Alternately, strategies may be envisioned for average-model converter implementation, particularly for loss-less models. Work at CAPS is proceeding with arithmetic functions of the injection currents. To accurately model the converter, in combination with its high-switching-frequency controller, the FPGA must read the firing pulse inputs, and the current functions must reflect the current switching state, the input current injections, and any necessary inductances. A schematic of the process model is shown in Figure 8.

To demonstrate the capability of the FPGA and the current injection function method, a notional DC-DC converter was implemented. The resultant model operates with a 2.27 $\mu$s time-step, and Figure 9 shows the microsecond-level voltage pattern that is a result of simulated controller switching.

6. CONCLUSION

The inclusion of an FPGA-based processor board into a real-time transient power simulation system has been implemented. Results have been shown from the power system co-simulation to demonstrate microsecond-level switching and control interaction.

7. ACKNOWLEDGEMENTS

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References
